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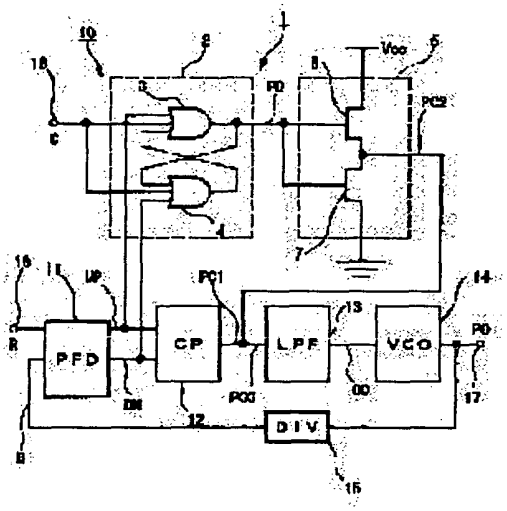
(54) PLL CIRCUIT USING CLOCK DITHERING CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a PLL circuit which uses a clock dithering circuit whose configuration is simple without being limited by the frequency division ratio of a feedback frequency divider.
SOLUTION: A clock dithering circuit 1 consisting of a storing means 2 and a charge pump circuit 5 is provided parallelly with a charge pump circuit 12. The means 2 stores phase difference signals UP and DN outputted by a phase comparator circuit 11 and generates a control signal PD whose level is inverted in accordance with the change of phase delay or advance. The circuit 5 generates a charge pump signal PC2 on the basis of the signal PD, supplies it to a low pass filter 13 and generates fluctuation of a constant period in an output frequency.



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